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Microprocessor Utilization in Search & Rescue Missions

FINAL REPORT

Introduction:

The position of an emergency transmitter may be determined by measuring the Doppler shift of the distress signal as received by an orbiting satellite. This requires the computation of an initial estimate and refinement of this estimate through an iterative, nonlinear, least-squares estimation.

A version of the above algorithm was implemented at Goddard Space Flight Center (GSFC) and tested by locating a transmitter on the premises and obtaining observations from a satellite. The computer used was an IBM 360/95. The position was determined within the desired 10 km radius accuracy.

The purpose of this project is to determine the feasibility of performing the same task in real time using microprocessor technology. The least square algorithm was implemented on an Intel 8080 microprocessor and the same experiment was run as at GSFC.

The results indicate that a microprocessor can easily match the IBM implementation in accuracy and be performed inside the time limitations set.

(NASA-CR-156746) MICROPROCESSOR UTILIZATION
IN SEARCH AND RESCUE MISSIONS Final Report
(Columbia Univ.) 47 p HC A03/MF A01

N78-22749

CSCL 09B

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National Aeronautics
Computer Science & Space Administration
Greenbelt, MD. 20771



DEC 27 1977

Why Microprocessors:

Time is an implicit restriction in any search and rescue mission. The use of satellites and computers is dictated by that time limit. The use of a big computer to determine the position presupposes communication between the satellite and the computer. This communication introduces a time delay since the satellite is not always within radio visibility of an installation that possesses both the communication and computing power for this problem. Furthermore the result has to be forwarded to a command center to do the dispatching.

Microprocessor utilization can alleviate this situation in two ways: by giving cheap computing power to communication facilities or by incorporating the computing power in the satellite itself thus eliminating this communication completely.

Microprocessors offer light weight, small volume, low power processing. Their speed is improving rapidly and their cost is going down. They are the logical choice for a satellite search and rescue system if they can perform.

Machine Configuration:

Strictly speaking there are three microprocessor configurations in this project which we are going to discuss individually.

- Development system
- Minimal execution system
- Actual field configuration

Initially our development system consisted of an MDS-80 Inteltec micro-computer by Intel with 16k bytes of RAM memory and a resident ROM monitor. Most of the floating point package was developed in machine language on that system using the monitor's limited hexadecimal editor and debugger. The need for more sophistication became apparent. After several failures in exploring alternatives (as fancy as hooking up to a PDP 11 through a telephone line for more storage) we were able to acquire a dual floppy disk drive by Intel. A spare line printer was attached to the system with minor hardware modifications and 16k bytes more RAM were added in order to support DOS. The enhanced system had the power of a mini-computer in software (assembler, editor, library manager, linkage editor, loader, and a sufficient file manager) at a speed which was slow but acceptable. The floating point package was converted to assembly language, and two more packages were developed: the I/O package and the matrix manipulation package. Unexpected help came from the use of ICE-80 (In Circuit Emulator), designed for a different application, as a powerful symbolic debugger substituting for the monitor hexadecimal debugger.

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- The CPU card
- 16k Bytes of memory

- The console device and its interface
- Power supply: 12V, 5V, -5V, ground

Additionally, the line printer was used to produce a hardcopy version of the results.

The actual field configuration would be the same if the machine were located on the ground. Some kind of communications equipment would be required to provide the data input and, maybe, start the run automatically. The configuration would be different, though, if the machine were located on the satellite. The requirements for the satellite configuration would be:

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The Floating Point Package:

Based on estimates of the number of operations required we were inclined to think that any floating point operations would have to be performed by hardware and not by software since estimated times became prohibitive. This floating point package was developed to help us count the actual number of operations rather than perform them in an actual situation. The final run proved our estimates wrong and the package gained new importance.

There are a number of representations of floating point numbers differing in accuracy and range as a trade off to the number of bytes required per number. The one used was the ANSI format for FORTRAN which happens to be implemented by hardware as an option in IBM computers. It consists of one sign bit, a seven bit exponent (excess 64), and a 24 bit mantissa of hexadecimal digits. The accuracy is 6 hexadecimal digits or approximately 7.2 decimal digits. Specific operations were not timed although a more general timing analysis appears in a later section. This format was chosen as opposed to the BCD format because the space requirements are lower for the same amount of precision, which in turn reduces execution time slightly. A mantissa of binary digits was not used because of the frequent need for normalization.

Addition and subtraction take exactly the same time, whereas multiplication is approximately equal to 22 addition and division is approximately 60 additions.

Multiplication produces a 48 bit result mantissa which is then normalized and rounded to 24 bits. This preserved the number of significant digits, or, viewed from a different angle, is the same as a double precision multiply if the two arguments were expanded with zero fill.

Division preserves the significant digits again by expanding the mantissa of the dividend to double precision and results in full single precision result. Normalization and rounding occur as in multiplication.

Accuracy is thus preserved to true single precision throughout in a numerically stable manner keeping the length of the number to 4 bytes. The cost is expensive multiplication and, especially, division. This dictates a programming style whereby division is avoided unless it is absolutely necessary. The benefits, on the other hand, are numerically stable implementations whose results match the double precision to the extent possible as will be seen when the results of the run are analyzed.

The square root function was implemented by using a variation of Heron's formula based on the observation that the mantissa of any floating point number will have a value of $1/16$ to 1 (interpreted as a fraction). As a first guess an approximation to a straight line connecting the two end points is made. Experimentally, six iterations were found necessary to produce an accurate result. A better first guess could improve that significantly, but time constraints did not allow us to pursue that direction.

Finally, input and output of floating point numbers turn out a much more serious task than first expected. The input routine recognized numbers with a maximum of ten integer and ten fraction digits. This proved more than sufficient for our needs. The output routine produces a rigid scientific format with 10 fraction digits. When interpreting the results it should be kept in mind that at most only 7 are significant. The format was retained in case of future expansion of the mantissa. Both the input and output routines could be better, but since their function is only tangential to the project at hand they were kept on the bare functional level.

Matrix Operations:

All matrices in the system are defined as two dimensional, including vectors. The first two bytes contain the number of rows and the number of columns in the particular matrix, respectively. This effectively limits the number of observations to 256. Vectors have one of their dimensions identically equal to 1. The next two bytes contain the address of the first byte that follows the last byte belonging to the matrix. Adjacent elements in a row of the matrix are stored as adjacent floating point numbers in memory. Rows are stored sequentially starting from the first row in the fifth byte.

In an effort to minimize the number of address calculations in the least squares algorithm the APL program we were supplied with, (LSQ), was converted into FORTRAN. The calculations involved in the residual equations were all grouped together inside one big loop. The advantage of such a scheme is that once an offset is calculated it can be used to address all the needed elements of the matrices involved in the calculation. When the time came though, to implement it using 8080 assembly language, it became all too apparent that there were too many addresses to keep track of and too few registers to help. Therefore, due to the limitation of addressing capabilities, routines were implemented for the various matrix operators in APL. This resulted in well structured and very efficient code, the style being dictated by the instruction set.

A minimum number of matrix utility routines was necessary. Matrices can be created by specifying their dimensions, they can be filled with zeros, they can be read from a device, they can be moved (copied) in storage.

There are four classes of operations by which matrices may be altered involving the following arguments.

- a constant and a matrix
- a vector and a matrix

- two matrices (plus possibly a result matrix)
- one matrix (for example, inversion)

In our particular application there was only one inversion of a 2 by 2 matrix involved. A simple algorithm derived from Euler's method is implemented using fixed pivots. Execution time and temporary storage are optimized.

Implementing the Experiment:

Having developed the tools that were discussed in previous sections the actual implementation was straight forward. For reasons already mentioned a routine was written to match the ISQ routine* developed by Dr. Marini almost statement by statement. The correspondence is indicated in the source program by keeping track of the APL statement numbers. The array names were kept the same as much as possible and only one additional temporary matrix was required. The program was written for a maximum of 100 observations. All matrix operations as well as the square root keep track of the calls to the floating point routines.

The whole package makes limited use of two monitor routines, which can easily be eliminated. The reason they are there is because software was being developed in machine language and the monitor provided a lot of needed help. So, essentially, ISQ can be run completely independently.

The space requirements for this particular run was approximately 16k bytes, out of which 4k could be in ROM and 12k in RAM. The exact numbers are as follows:

Code:	3656 bytes
Data:	10365 bytes
Stack:	100 bytes (arbitrarily)
Total:	14121 bytes

Incorporated into the package were four counting routines that kept track of the number of additions, subtractions, multiplications and divisions required during each iteration. The results will be analyzed in the next section. The actual implementation would not require these routines. The counting overhead to each arithmetic operation is approximately equal to half the time of an addition.

* See Appendix C.

Interpreting the Results:

The final run converged and yielded five digits of accuracy. If convergence is defined as a ratio of two successive RMS residuals being close to 1 (in absolute) it was attained at the ninth iteration to within 0.00001. Comparing these results to the run at GSFC (run at double precision, or 16 digits of accuracy) we note the 5 digit accuracy of our result.

Numerical analysis gives us enough tools to justify the loss of two significant digits in the course of the iterations. The main source of error appears to be the subtraction of the estimated range rates from the actuals. The subtraction of the average residual equations could contribute to the error as well.

The measured execution time for this particular run was 62 seconds per iteration. The microprocessor used was an 8080A by Intel. Adjusting for counting the number of operations the true time becomes 61 seconds. The 8080A CPU has a cycle time of 2 microseconds. If this system were actually implemented, the 8080A-1 CPU could be used which offers higher speed with cycle time of 1.3 microseconds which could bring execution time down to 40 seconds for each iteration giving approximately 6 minutes to reach convergence. This figure is derived with no modification of the software. Since it falls within our definition of "real time", which was around 15 minutes, it is definitely a workable solution.

Another alternative is, of course, to use hardware floating point units. Two units that we are familiar with indicate a disparity in execution times of several orders of magnitude. Their specifications appear in Appendix B for the purposes of the following analysis, 'typical' execution times for 8 digits of precision of the North Star Computers, Inc. FPB unit were used. Our system indicated the following frequency of floating point operations for each iteration:

Subtractions - 672

Multiplications - 2382

Divisions - 940

When trying to compute the time it would take to execute those instructions we noticed that the time it takes to access hardware floating point unit is more than twice than the time it takes to do the calculations. Namely, we came up with the following numbers:

<u>TIME</u> (SEC)	<u>PURPOSE</u>
0.35	perform the operations
0.825	input and output the number form FPB (8080A-1)
1.175	total time required

Therefore, use of hardware units make it possible to decrease the execution time by one order of magnitude.

Future Research:

The parameters that have to be optimized in the search and rescue mission consist of the accuracy of the position estimation and the time in which it is performed. Proving the feasibility of a microprocessor implementation is far from devising an optimal algorithm.

If the nonlinear regression method is utilized there is a lot of room for improvement in the initial estimate, a quantity that can affect the whole outcome of the iterations. Several methods that are suggested in Dr. Marini's paper can be explored. Furthermore, since the data collection takes an appreciable amount of time an algorithm should be devised in which an estimate is upgraded with each incoming datum. If that algorithm is good enough then the estimate could be the result itself.

A further enhancement on the calculation time can be achieved through parallelism. It can appear on two levels:

- The implementation of the least squares algorithm
- The grouping of data

The least squares algorithm may be broken into parallel subtasks that can be performed by different processors in parallel, especially floating point operations.

The data may be grouped in clusters on which the least squares algorithm is applied. The estimate provided by each cluster is then processed through least squares estimation itself. This method could be applied at data collection time too.

Appendix A

- Sample run at GSFC
- Sample run at Columbia

1 LSO E

DUALS: 1.050744637

HGT ARE: 42.3067512 261.49471

IS:

243245 -4693.396224 4270.874121

IRAS

475993

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1 LSO EN

DUALS: 0.1359538763

HGT ARE: 40.33781496 277.2125703 9.094947018E-13

IS:

20014 -4830.001894 4100.600277

IRAS

45525

1 LSO EN

DUALS: 0.07064076362

HGT ARE: 39.76197471 279.9200369 9.094947018E-13

IS:

25536 -4836.251765 4057.716223

IRAS

47161

1 LSO EN

DUALS: 0.06507914984

HGT ARE: 39.47765191 281.0748775 9.094947018E-13

IS:

24357 -4837.990343 4033.099034

IRAS

43854

1 LSO EN

DUALS: 0.06478401403

HGT ARE: 39.36049512 281.5253002 9.094947018E-13

IS:

22331 -4838.305495 4023.05154

IRAS

44862

1 LSO EN

DUALS: 0.06474873470

HGT ARE: 39.32402904 281.6773949 0

IS:

2299 -4838.366335 4020.220503

IRAS

43943

1 LSO EN

DUALS: 0.06478068825

HGT ARE: 39.31537952 281.7107637 0

IS:

23076 -4838.378943 4019.477604

IRAS

44357

1 LSO EN

DUALS: 0.06474004010

HGT ARE: 39.31352503 281.7179045 0

IS:

23075 -4838.381637 4019.218311

IRAS

1. L50 EN
13. RESIDUALS: 0.06474804013
14. L50 HGT ARE: 39.31352503 201.7122041 0
15. POSITION 15:
16. 27575 74838.381637 4019.318311
17. 118
18. 27575 74838.381637 4019.318311

1. L50 EN
13. RESIDUALS: 0.06474803883
14. L50 HGT ARE: 39.31303801 201.7197720 0
15. POSITION 15:
16. 27575 74838.382347 4019.276473
17. 118
18. 27575 74838.382347 4019.276473

1. L50 EN
13. RESIDUALS: 0.06474803883
14. L50 HGT ARE: 39.31303448 201.7197324 0
15. POSITION 15:
16. 27575 74838.382353 4019.276175
17. 118
18. 27575 74838.382353 4019.276175

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THE RESULTING POSITION IS: sample run at Columbia
X= -0.5534835815E+03 Y= -0.4828028678E+04 Z= 0.4393360137E+04

RMS RESIDUALS = 0.1154615402E+01

THE RESULTING POSITION IS:

X= 0.6216947555E+03 Y= -0.4912517547E+04 Z= 0.4176822662E+04

RMS RESIDUALS = 0.1050682067E+01

THE RESULTING POSITION IS:

X= 0.8464587211E+03 Y= -0.4839673995E+04 Z= 0.4060588836E+04

RMS RESIDUALS = 0.1389477729E+00

THE RESULTING POSITION IS:

X= 0.2470703125E+03 Y= -0.4838634490E+04 Z= 0.4033941268E+04

RMS RESIDUALS = 0.0706402111E+00

THE RESULTING POSITION IS:

X= 0.9875150680E+03 Y= -0.4838407516E+04 Z= 0.4023446083E+04

RMS RESIDUALS = 0.0650796318E+00

THE RESULTING POSITION IS:

X= 0.9999647140E+03 Y= -0.4838378906E+04 Z= 0.4020233154E+04

RMS RESIDUALS = 0.0647644424E+00

THE RESULTING POSITION IS:

X= 0.1002853393E+04 Y= -0.4838379859E+04 Z= 0.4019498825E+04

RMS RESIDUALS = 0.0647490596E+00

THE RESULTING POSITION IS:

X= 0.1003520965E+04 Y= -0.4838384628E+04 Z= 0.4019325256E+04

RMS RESIDUALS = 0.0647480487E+00

THE RESULTING POSITION IS:

X= 0.1003620147E+04 Y= -0.4838379859E+04 Z= 0.4019290460E+04

RMS RESIDUALS = 0.0647478675E+00

THE RESULTING POSITION IS:

X= 0.1003682136E+04 Y= -0.4838384628E+04 Z= 0.4019283294E+04

RMS RESIDUALS = 0.0647482872E+00

THE RESULTING POSITION IS:

X= 0.1003667831E+04 Y= -0.4838379859E+04 Z= 0.4019290924E+04

RMS RESIDUALS = 0.0647483444E+00

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Appendix B

Two typical hardware floating point units

- FPB by North Star Computers, Inc.
- FPU by Cybernetic Micro Systems

FPB DATA SHEET

EXECUTION TIMES 1, 2, 3

PRECISION DIGITS:		2	4	6	8	10	12	14
ADD	best	1	1	1	1	1	1	1
	typical	8	8	9	9	10	10	11
	worst	10	10	10	11	11	12	12
SUBTRACT	best	4	4	4	4	4	4	4
	typical	8	8	9	9	10	10	11
	worst	15	16	17	18	19	20	21
MULTIPLY	best	5	5	5	5	5	5	5
	typical	18	34	55	80	111	146	186
	worst	51	125	228	382	527	720	933
DIVIDE	best	7	7	7	7	7	7	7
	typical	39	70	109	156	211	274	370
	worst	62	139	229	340	470	621	779

1. Times given in microseconds
2. Execution times are a function of the input values
3. Times listed do not include transmission of input values and result

Board dimensions:

Model A: 5 in. by 10 in.
Model B: 6 1/4 in. by 12 in.

Power requirements:

Model A: 8 V (unregulated) @ 1.7 A
Model B: 5 V (regulated) @ 1.7 A

Board Construction:

FR4 material, gold plated edge connectors

Floating point number representation:

Byte 1: bit 7 = sign (1 = negative number, 0 = positive number)
bits 6-0 = exponent in excess 64 binary representation
bits 7-0 = zero represents the zero value
Byte 2: bits 3-0 = least significant digit of value in BCD coding
bits 7-4 = next least significant digit of value
Byte n: bits 7-4 = most significant digit of value in BCD coding
bits 3-0 = next most significant digit of value
All values are normalized.

- *Sample use of the North Star FPB for a divide operation with 8 digit precision
- *In this example assume arguments are in memory in form:
 - Most significant byte (msb) digit pair
 - Susequent digit pairs follow the msb
 - Exponent/sign byte follows lsb digit pair.
 - Pointer addresses the exponent/sign byte
- *BC has left arg pointer
- *DE has right arg pointer
- *HL has result pointer
- *The FPB receives its arguments by "peeking" at the 8080 bus
- *when the argument values are loaded to accumulator.
- *Two jumperable "hardwired" addresses are required for signaling the FPB
- *This routine may be generalized to perform any operation, at any precision.

I DIV LDA RSTRT	This "hardwired" reference signals FPB to "wake up"
MVI A,8*16+DIVOP	Specify precision and operation code to FPB
LDAX D	Exponent/sign byte of right arg
DCX D	Advance pointer to next byte
LDAX D	Least significant digit pair of right arg
DCX D	Advance pointer to next byte
LDAX D	
DCX D	
LDAX D	
DCX D	
LDAX D	Most significant digit pair of right arg
LDAX B	Exponent/sign byte of left arg
DCX B	
LDAX B	Least significant digit pair of left arg
DCX B	
LDAX B	
DCX B	
LDAX B	
DCX B	
LDAX B	Most significant digit pair of left arg
• Now the Floating Point Board is performing the operation	
LXI D,FPDIN	"Hardwired" address for receiving value from FPB
FDIV1 LDAX D	Loop waiting for completion signal (sign bit)
ORA A	The FPB is done when the sign bit becomes "1"
JP FDIV1	Loop if sign bit is still "0"
ANI EBIT5	Check for error, condition tested at end
LDAX D	Exponent/sign of result
MOV M,A	Store exponent/sign of result
DCX H	Advance pointer.
LDAX D	Least significant digit pair of result
MOV M,A	
DCX H	
LDAX D	
MOV M,A	
DCX H	
LDAX D	
MOV M,A	
DCX H	
LDAX D	msb byte of result
MOV M,A	Store it
RZ	Return if no error was detected
JMP ERROR	Go report error (i.e. underflow or divide by 0)

FLOATING POINT UNIT

PRICE LIST

MODEL	QUANTITY		
	1	25	100
#1	\$595.00	\$535.00	\$475.00
#2	470.00	425.00	375.00
#3	345.00	315.00	275.00

All sales FOB Palo Alto

EXECUTION TIMES

FUNCTION	TIME IN MILLISECONDS (approximate)
ADD, SUB	110
MUL, DIV, SQRT	225
TAN	846
LN, SIN, COS, →POL	1250
POWER	1720

CYBERNETIC MICRO SYSTEMS
2460 EMBARCADERO WAY
PALO ALTO, CA 94303
(415) 321-0410

Appendix C

The APL least squares program

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Accuracy is thus preserved to true single precision throughout in a numerically stable manner keeping the length of the number to 4 bytes. The cost is expensive multiplication and, especially, division. This dictates a programming style whereby division is avoided unless it is absolutely necessary. The benefits, on the other hand, are numerically stable implementations whose results match the double precision to the extent possible as will be seen when the results of the run are analyzed.

The square root function was implemented by using a variation of Heron's formula based on the observation that the mantissa of any floating point number will have a value of $1/16$ to 1 (interpreted as a fraction). As a first guess an approximation to a straight line connecting the two end points is made. Experimentally, six iterations were found necessary to produce an accurate result. A better first guess could improve that significantly, but time constraints did not allow us to pursue that direction.

Finally, input and output of floating point numbers turn out a much more serious task than first expected. The input routine recognized numbers with a maximum of ten integer and ten fraction digits. This proved more than sufficient for our needs. The output routine produces a rigid scientific format with 10 fraction digits. When interpreting the results it should be kept in mind that at most only 7 are significant. The format was retained in case of future expansion of the mantissa. Both the input and output routines could be better, but since their function is only tangential to the project at hand they were kept on the bare functional level.

Matrix Operations:

All matrices in the system are defined as two dimensional, including vectors. The first two bytes contain the number of rows and the number of columns in the particular matrix, respectively. This effectively limits the number of observations to 256. Vectors have one of their dimensions identically equal to 1. The next two bytes contain the address of the first byte that follows the last byte belonging to the matrix. Adjacent elements in a row of the matrix are stored as adjacent floating point numbers in memory. Rows are stored sequentially starting from the first row in the fifth byte.

In an effort to minimize the number of address calculations in the least squares algorithm the APL program we were supplied with, (LSQ), was converted into FORTRAN. The calculations involved in the residual equations were all grouped together inside one big loop. The advantage of such a scheme is that once an offset is calculated it can be used to address all the needed elements of the matrices involved in the calculation. When the time came though, to implement it using 8080 assembly language, it became all too apparent that there were too many addresses to keep track of and too few registers to help. Therefore, due to the limitation of addressing capabilities, routines were implemented for the various matrix operators in APL. This resulted in well structured and very efficient code, the style being dictated by the instruction set.

A minimum number of matrix utility routines was necessary. Matrices can be created by specifying their dimensions, they can be filled with zeros, they can be read from a device, they can be moved (copied) in storage.

There are four classes of operations by which matrices may be altered involving the following arguments.

- a constant and a matrix
- a vector and a matrix

- two matrices (plus possibly a result matrix)
- one matrix (for example, inversion)

In our particular application there was only one inversion of a 2 by 2 matrix involved. A simple algorithm derived from Euler's method is implemented using fixed pivots. Execution time and temporary storage are optimized.

Implementing the Experiment:

Having developed the tools that were discussed in previous sections the actual implementation was straight forward. For reasons already mentioned a routine was written to match the LSQ routine* developed by Dr. Marini - 1 most statement by statement. The correspondence is indicated in the source program by keeping track of the APL statement numbers. The array names were kept the same as much as possible and only one additional temporary matrix was required. The program was written for a maximum of 100 observations. All matrix operations as well as the square root keep track of the calls to the floating point routines.

The whole package makes limited use of two monitor routines, which can easily be eliminated. The reason they are there is because software was being developed in machine language and the monitor provided a lot of needed help. So, essentially, LSQ can be run completely independently.

The space requirements for this particular run was approximately 16k bytes, out of which 4k could be in ROM and 12k in RAM. The exact numbers are as follows:

Code: 3656 bytes
Data: 10365 bytes
Stack: 100 bytes (arbitrarily)
Total: 14121 bytes

Incorporated into the package were four counting routines that kept track of the number of additions, subtractions, multiplications and divisions required during each iteration. The results will be analyzed in the next section. The actual implementation would not require these routines. The counting overhead to each arithmetic operation is approximately equal to half the time of an addition.

* See Appendix C.

Interpreting the Results:

The final run converged and yielded five digits of accuracy. If convergence is defined as a ratio of two successive RMS residuals being close to 1 (in absolute) it was attained at the ninth iteration to within 0.00001. Comparing these results to the run at GSFC (run at double precision, or 16 digits of accuracy) we note the 5 digit accuracy of our result.

Numerical analysis gives us enough tools to justify the loss of two significant digits in the course of the iterations. The main source of error appears to be the subtraction of the estimated range rates from the actuals. The subtraction of the average residual equations could contribute to the error as well.

The measured execution time for this particular run was 62 seconds per iteration. The microprocessor used was an 8080A by Intel. Adjusting for counting the number of operations the true time becomes 61 seconds. The 8080A CPU has a cycle time of 2 microseconds. If this system were actually implemented, the 8080A-1 CPU could be used which offers higher speed with cycle time of 1.3 microseconds which could bring execution time down to 40 seconds for each iteration giving approximately 6 minutes to reach convergence. This figure is derived with no modification of the software. Since it falls within our definition of "real time", which was around 15 minutes, it is definitely a workable solution.

Another alternative is, of course, to use hardware floating point units. Two units that we are familiar with indicate a disparity in execution times of several orders of magnitude. Their specifications appear in Appendix B for the purposes of the following analysis, 'typical' execution times for 8 digits of precision of the North Star Computers, Inc. FPB unit were used. Our system indicated the following frequency of floating point operations for each iteration:

Subtractions - 672

Multiplications - 2382

Divisions - 940

When trying to compute the time it would take to execute those instructions we noticed that the time it takes to access hardware floating point unit is more than twice than the time it takes to do the calculations. Namely, we came up with the following numbers:

<u>TIME</u> (SEC)	<u>PURPOSE</u>
0.35	perform the operations
0.825	input and output the number form FPB (8080A-1)
1.175	total time required

Therefore, use of hardware units make it possible to decrease the execution time by one order of magnitude.

Future Research:

The parameters that have to be optimized in the search and rescue mission consist of the accuracy of the position estimation and the time in which it is performed. Proving the feasibility of a microprocessor implementation is far from devising an optimal algorithm.

If the nonlinear regression method is utilized there is a lot of room for improvement in the initial estimate, a quantity that can affect the whole outcome of the iterations. Several methods that are suggested in Dr. Marini's paper can be explored. Furthermore, since the data collection takes an appreciable amount of time an algorithm should be devised in which an estimate is upgraded with each incoming datum. If that algorithm is good enough then the estimate could be the result itself.

A further enhancement on the calculation time can be achieved through parallelism. It can appear on two levels:

- The implementation of the least squares algorithm
- The grouping of data

The least squares algorithm may be broken into parallel subtasks that can be performed by different processors in parallel, especially floating point operations.

The data may be grouped in clusters on which the least squares algorithm is applied. The estimate provided by each cluster is then processed through least squares estimation itself. This method could be applied at data collection time too.

Appendix A

- Sample run at GSFC
- Sample run at Columbia

1 L80 E

DUALS: 1.050744637

HGT ARE: 42.3067070 1.050744637 0

ON 18:

-4693.396224 1270.87121

1195

11993

1 L80 EN

DUALS: 0.1369538700

HGT ARE: 40.33781496 277.2129723 9.094947018E-13

ON 18:

-4830.001894 4186.660277

1195

11925

1 L80 EN

DUALS: 0.07964076362

HGT ARE: 39.76197471 279.9200369 9.094947018E-13

ON 18:

-4836.251765 4657.716223

1195

11161

1 L80 EN

DUALS: 0.06507914984

HGT ARE: 39.47765191 281.0740373 9.094947018E-13

ON 18:

-4837.900343 4633.019834

1195

11354

1 L80 EN

DUALS: 0.06476461400

HGT ARE: 39.35049512 281.0032507 9.094947018E-13

ON 18:

-4838.305495 4029.35154

1195

11362

1 L80 EN

DUALS: 0.06474370477

HGT ARE: 39.32402504 281.6773249 0

ON 18:

-4838.366335 4029.220503

1195

11343

1 L80 EN

DUALS: 0.06474206880

HGT ARE: 39.31537252 281.7107637 0

ON 18:

-4838.378993 4019.477504

1195

11357

1 L80 EN

DUALS: 0.06474004017

HGT ARE: 39.31032503 281.7172045 0

ON 18:

-4838.381637 4019.118311

1195

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EN

161 PRE: 39.31503801 201.7137750 0

238

709 -4838.382347 40519.276422

10

152

150. END

URL: 0.00474803883

OGT ARE: 39.31303448 201.1192224 34

1 2 3

1995 -4838.382353 -4919.234175

100

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THE RESULTING POSITION IS:
X= +0.5034835815E+03 Y= -0.4828028678E+04 Z= 0.4393360137E+04

RMS RESIDUALS = 0.1154615402E+01

THE RESULTING POSITION IS:

X= 0.6216947555E+03 Y= -0.4912517547E+04 Z= 0.4176822662E+04

RMS RESIDUALS = 0.1050682067E+01

THE RESULTING POSITION IS:

X= 0.8464587211E+03 Y= -0.4839673995E+04 Z= 0.4060588836E+04

RMS RESIDUALS = 0.1389477729E+00

THE RESULTING POSITION IS:

X= 0.9470703125E+03 Y= -0.4829634496E+04 Z= 0.4033941268E+04

RMS RESIDUALS = 0.0706402111E+00

THE RESULTING POSITION IS:

X= 0.9875150680E+03 Y= -0.4838407516E+04 Z= 0.4023446083E+04

RMS RESIDUALS = 0.0650796318E+00

THE RESULTING POSITION IS:

X= 0.999647140E+03 Y= -0.4838378906E+04 Z= 0.4020233154E+04

RMS RESIDUALS = 0.0647644424E+00

THE RESULTING POSITION IS:

X= 0.1002853393E+04 Y= -0.4838379859E+04 Z= 0.4019498825E+04

RMS RESIDUALS = 0.0647490596E+00

THE RESULTING POSITION IS:

X= 0.1003526965E+04 Y= -0.4838384628E+04 Z= 0.4019325256E+04

RMS RESIDUALS = 0.0647486487E+00

THE RESULTING POSITION IS:

X= 0.1003620147E+04 Y= -0.4838379859E+04 Z= 0.4019300450E+04

RMS RESIDUALS = 0.0647478675E+00

THE RESULTING POSITION IS:

X= 0.1003682136E+04 Y= -0.4838384628E+04 Z= 0.4019283294E+04

RMS RESIDUALS = 0.0647482872E+00

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THE RESULTING POSITION IS:

X= 0.1003667821E+04 Y= -0.4838379859E+04 Z= 0.4019290934E+04

RMS RESIDUALS = 0.0647483444E+00

Appendix B

Two typical hardware floating point units

- FPB by North Star Computers, Inc.
- FPU by Cybernetic Micro Systems

FPB DATA SHEET

EXECUTION TIMES 1, 2, 3

PRECISION DIGITS:		2	4	6	8	10	12	14
ADD	best	1	1	1	1	1	1	1
	typical	8	8	9	9	10	10	11
	worst	10	10	10	11	11	12	12
SUBTRACT	best	4	4	4	4	4	4	4
	typical	8	8	9	9	10	10	11
	worst	15	16	17	18	19	20	21
MULTIPLY	best	5	5	5	5	5	5	5
	typical	18	34	55	80	111	146	186
	worst	51	125	228	382	527	720	933
DIVIDE	best	7	7	7	7	7	7	7
	typical	39	70	109	156	211	274	370
	worst	62	139	229	340	470	621	779

1. Times given in microseconds
2. Execution times are a function of the input values
3. Times listed do not include transmission of input values and result

Board dimensions:

Model A: 5 in. by 10 in.

Model B: 6 1/4 in. by 12 in.

Power requirements:

Model A: 8 V (unregulated) @ 1.7 A

Model B: 5 V (regulated) @ 1.7 A

Board Construction:

FR4 material, gold plated edge connectors

Floating point number representation:

Byte 1: bit 7=sign (1=negative number, 0=positive number)

bits 6-0 = exponent in excess 64 binary representation

bits 7-0 = zero represents the zero value

Byte 2: bits 3-0 = least significant digit of value in BCD coding

bits 7-4 = next least significant digit of value

Byte n: bits 7-4 = most significant digit of value in BCD coding

bits 3-0 = next most significant digit of value

All values are normalized.

Other representations of BCD floating point numbers require a change in microcode and are available on special order.

- *Sample use of the North Star FPB for a divide operation with 8 digit precision
- *In this example assume arguments are in memory in form:
 - * Most significant byte (msb) digit pair
 - * Susequent digit pairs follow the msb
 - * Exponent/sign byte follows lsb digit pair.
 - * Pointer addresses the exponent/sign byte
- *BC has left arg pointer
- *DE has right arg pointer
- *HL has result pointer

- *The FPB receives its arguments by "peeking" at the 8080 bus
- *when the argument values are loaded to accumulator.
- *Two jumperable "hardwired" addresses are required for signaling the FPB
- *This routine may be generalized to perform any operation, at any precision.

FDIV LDA RSTR	This "hardwired" reference signals FPB to "wake up"
MVI A,8*16+DIVOP	Specify precision and operation code to FPB
LDAX D	Exponent/sign byte of right arg
DCX D	Advance pointer to next byte
LDAX D	Least significant digit pair of right arg
DCX D	Advance pointer to next byte
LDAX D	
DCX D	
LDAX D	
DCX D	
LDAX D	Most significant digit pair of right arg
LDAX B	Exponent/sign byte of left arg
DCX B	
LDAX B	Least significant digit pair of left arg
DCX B	
LDAX B	
DCX B	
LDAX B	
DCX B	
LDAX B	Most significant digit pair of left arg
* Now the Floating Point Board is performing the operation	
LXI D,FPDIN	"Hardwired" address for receiving value from FPB
FDIV1 LDAX D	Loop waiting for completion signal (sign bit)
ORA A	The FPB is done when the sign bit becomes "1"
JP FDIV1	Loop if sign bit is still "0"
ANI EBITS	Check for error, condition tested at end
LDAX D	Exponent/sign of result
MOV M,A	Store exponent/sign of result
DCX H	Advance pointer.
LDAX D	Least significant digit pair of result
MOV M,A	
DCX H	
LDAX D	
MOV M,A	
DCX H	
LDAX D	msb byte of result
MOV M,A	Store it
RZ	Return if no error was detected
JMP ERROR	Go report error (i.e. underflow or divide by 0)

FLOATING POINT UNIT

PRICE LIST

MODEL	QUANTITY		
	1	25	100
#1	\$595.00	\$535.00	\$475.00
#2	470.00	425.00	375.00
#3	345.00	315.00	275.00

All sales FOB Palo Alto

EXECUTION TIMES

FUNCTION	TIME IN MILLISECONDS (approximate)
ADD, SUB	110
MUL, DIV, SQRT	225
TAN	846
LN, SIN, COS, →POL	1250
POWER	1720

CYBERNETIC MICRO SYSTEMS
2460 EMBARCADERO WAY
PALO ALTO, CA 94303
(415) 321-0410

Appendix C

The APL least squares program

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